AMENDMENTS TO THE CLAIMS

Please amend claims 1, 2, 4, 5, 8, 10, and 11, and add new claims 13-23, to read as follows:

1. (Currently amended) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;

a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern;

a scan mode terminal providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and

reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode ~~in accordance with a~~, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

2. (Currently amended) The semiconductor integrated circuit according to Claim 1, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal.

3. (Original) The semiconductor integrated circuit according to Claim 2, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode.

4. (Currently amended) The semiconductor integrated circuit according to Claim 3, further comprising:

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode ~~in accordance with~~ responsive to said mode signal.

5. (Currently amended) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry ~~comprising:~~ as set forth in claim 1, wherein ~~a~~ said plurality of flip-flops are serially arranged so as to perform scan testing for said internal logical circuitry; and

said reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode ~~in accordance with a~~ responsive to said mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

6. (Original) The semiconductor integrated circuit according to Claim 1, further comprising transition detection means for detecting the transition timing of said logical level of said

mode signal, wherein said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

7. (Original) The semiconductor integrated circuit according to Claim 5, further comprising transition detection means for detecting the transition timing of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

8. (Currently amended) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 1, wherein ~~,~~ ~~comprising:~~

~~a plurality of flip-flops serially arranged so as to perform scan testing for said internal logical circuitry; and~~

~~output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode, while prohibiting the outputting of data that is supplied during said normal operation mode~~said reset control means obtains an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal .

9. (Original) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry;

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

10. (Currently amended) A method of testing a semiconductor integrated circuit as defined in claim 1, ~~which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing~~, wherein

said plurality of flip-flops are reset when transitioning from said normal operation mode to said test mode.

11. (Currently amended) A method of testing a semiconductor integrated circuit as defined in claim 6, ~~which has internal logical circuitry and a plurality of flip-flops for scan testing said internal logical circuitry, and which has a normal operation mode and a test mode for performing said scan testing,~~ wherein

said plurality of flip-flops are reset when transitioning from said test mode to said normal operation mode.

12. (Original) A method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and memory means connected to said plurality of flip-flops, and which has a normal operation mode and a test

mode for performing said scan testing, wherein access to said memory means is prohibited during said test mode.

13. (New) The semiconductor integrated circuit as set forth in claim 1 further including a dummy flip-flop in said scan chain that is responsive to a rising and falling of the scan mode signal for resetting said scan flip-flops.

14. (New) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;

a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern;

a scan mode input providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and

reset means for resetting said plurality of flip-flops when transitioning from said normal operation mode to said test mode responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,

wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops when transitioning from said test mode to said normal operation mode in accordance with said mode signal, and further comprising

output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode, and

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

15. (New) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 14, wherein said plurality of flip-flops are arranged so as to perform scan testing for said internal logical circuitry; and

said reset means for resetting said plurality of flip-flops when transitioning from said test mode to said normal operation mode [in accordance with a] responsive to said mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

16. (New) The semiconductor integrated circuit according to Claim 14, further comprising transition detection means for detecting the transition timing of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

17. (New) The semiconductor integrated circuit according to Claim 15, further comprising transition detection means for detecting the transition timing of said logical level of said

mode signal, wherein said reset means resets said plurality of flip-flops when said transition timing detection means detects said transition timing.

18. (New) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 15, wherein said reset control means obtains an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

19. (New) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry;

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

20. (New) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a scan path between a scan in source receiving a scan pattern and a scan output with a scan chain including a plurality of scan flip-flops formed between said scan in source and the scan output, said scan flip-flops configured to make scan testing possible according to said scan pattern;

a scan mode signal provided for switching said internal logic circuitry between said normal operation mode and said test mode responsive to said scan mode signal;

a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect transition timing of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein

scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations.

21. The semiconductor circuit as set forth in claim 20, further including a dummy flip-flop in said scan path.

22. The semiconductor circuit as set forth in claim 20, wherein, during scan testing, said scan pattern is inputted to the scan flip-flops so that by a shift out of said scan chain, data that is to be checked for scan testing are shifted out from the scan output.

23. The semiconductor circuit as set forth in claim 20, wherein said reset control block includes a pair of flip-flops and logical output circuits arranged to detect transition timing of a logical level of the scan mode signal.